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(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
7 March 2002 (07.03.2002)

PCT

(10) International Publication Number
WO 02/19556 A2

- (51) International Patent Classification⁷: **H04B 1/707**
- (21) International Application Number: PCT/EP01/09930
- (22) International Filing Date: 27 August 2001 (27.08.2001)
- (25) Filing Language: English
- (26) Publication Language: English
- (30) Priority Data:
09/649,672 28 August 2000 (28.08.2000) US
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- (81) Designated States (*national*): CN, JP, KR.
- (84) Designated States (*regional*): European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR).
- Published:**
— *without international search report and to be republished upon receipt of that report*
- For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.*
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WO 02/19556 A2

(54) Title: TRACKING OF A MULTI-PATH RESOLVED SIGNAL IN A RAKE RECEIVER

(57) Abstract: A resolved component of a multi-path signal is assigned to a rake finger of a spread spectrum rake receiver. The resolved component is variably delayed. On the variably delayed resolved component, an early-late detection is performed so as to determine whether the resolved component arrived early or late with respect to an optimum arrival time. A first pulse is generated if said early-late detection determines that said resolved component arrived early. A second pulse is generated if said early-late detection determines that said resolved component arrived late. The first and second pulses and second pulses are counted. The first pulse causes counting in a first direction and the second pulse causes counting in a second direction. From the counting, a fractional-chip delay timing adjustment signal is derived, and fed back to adjust the variably delaying of the resolved component. Also from the counting a chip delay phase adjustment signal is derived, and fed back to control a phase of a pseudo-noise generator.

Tracking of a multi-path resolved signal in a rake receiver

The present invention relates to a method of tracking a resolved component of a multi-path signal assigned to a rake finger of a spread spectrum rake receiver, more particularly to such a rake receiver included in a spread spectrum communication device such as a CDMA handset.

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Cellular communication systems are well known. Such cellular communication systems comprise cells or radio zones, together covering a given geographical area. The cells include base stations that, through control and communication channels, establish and maintain communication links with mobile communication devices that are comprised in the system, and communicate with the mobile communication devices through established communication links.

One type of a cellular communication system is a so-called Direct Sequence CDMA (Code Division Multiple Access) spread spectrum system. In such a CDMA spread spectrum system, in addition to a transmitter, the mobile communication device typically has a so-called rake receiver with a number of rake fingers to resolve components of a multi-path received spread spectrum signal and to diversity combine resolved components so as to improve the signal-to-noise ratio of the received signal. The spread spectrum signals are received from transmitters that spread data signals over a frequency band by using spreading sequences. Elements in such a sequence are so-called chips. For spreading different data signals at different transmitters Walsh sequences are used for channelization and pseudo-noise-spreading sequences are used for scrambling. The rake receiver regenerates a data signal from a received spread spectrum signal by de-scrambling it with the same pseudo-noise sequence and by de-spreading it thereafter with the same Walsh sequence that was used to spread the data signal, and diversity combines multi-path received signals that originate from the same data signal. The rake receiver needs to initially synchronize to the transmitter from which it wants to receive a data signal. During such initial synchronization, a searcher comprised in the rake receiver resolves components of a multi-path-received signal, the components originating from the wanted data signal. Thereafter, the rake receiver adopts a

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tracking mode synchronization to keep the rake fingers synchronized to the resolved components that originate from the same wanted data signal. During tracking mode synchronization the rake fingers are kept aligned with their resolved components.

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It is an object of the invention to provide a rake receiver in which during tracking mode synchronization the rake fingers are kept aligned with their resolved components of a multi-path signal while using simple alignment means.

It is another object of the invention to provide a rake receiver with alignment
10 means that require a limited amount of memory.

It is still another object of the invention to provide a rake receiver with reduced power consumption.

In accordance with the invention, a method of tracking a resolved component of a multi-path signal assigned to a rake finger of a spread spectrum rake receiver is
15 provided, said method comprising:

- variably delaying said resolved component;
- performing an early-late detection on said variably delayed resolved component so as to determine whether said resolved component arrived early or late with respect to an optimum arrival time, and generating a first pulse if said early-late detection determines
20 that said resolved component arrived early and generating a second pulse if said early-late detection determines that said resolved component arrived late;
- counting said first and second pulses, said first pulse causing counting in a first direction and said second pulse causing counting in a second direction;
- deriving from said counting a fractional-chip delay timing adjustment signal, and feeding
25 back said derived fractional-chip delay timing adjustment signal to adjust said variably delaying of said resolved component, and
- deriving from said counting a chip delay phase adjustment signal, and feeding back said derived chip delay phase adjustment signal to control a phase of a pseudo-noise generator.

30 The invention is based upon the insight that by distributing multi-path alignment over timing alignment of a variable delay and phase alignment of the pseudo-noise generator, a simple variable delay arrangement may be used to provide the variable delay.

In an embodiment, a shift register implements the variable delay. Due to the invention, the shift register may be made very short and typically has only eight sections.

Advantageously, at least part of the variable delay is obtained as a bulk delay of an adjustable digital filter. Herewith, the length of the shift register may even be further reduced to typically two or four samples per chip. Reduction of samples, and thereby clock rates in the receiver, and reduction of complexity achieves reduced power consumption and reduced chip area. The delay of the digital filter may be adjusted by selecting filter coefficients from a look-up table, entries of the look-up table comprising filter coefficients representing predetermined delays.

In an embodiment, counters do counting of pulses generated by early-late detection. A first counter counts the pulses so as to obtain the fractional-chip delay timing adjustment signal, and, at chip boundary, provides a carry signal to a second counter. The second counter provides the chip delay phase adjustment signal to control a phase of the pseudo-noise generator.

Figure 1 schematically shows a CDMA spread spectrum system.

Figure 2 shows resolved components of a multi-path signal, and early/late signals.

Figure 3 shows a communication device with a rake finger in such a rake receiver, according to the invention.

Figure 4 shows an early/late detector in a rake finger of a mobile communication device according to the invention.

Figure 5 shows a counter arrangement in a rake finger according to the invention.

Figure 6 shows an adjustable digital FIR filter in a rake finger according to the invention.

Figure 7 shows a look-up table with filter tap coefficients for a FIR filter.

Figure 8 shows a controllable shift register in a rake finger according to the invention.

Throughout the figures the same reference numerals are used for the same features.

Figure 1 schematically shows a CDMA spread spectrum system 1. The system 1 comprises radio zones 2-8, each respectively comprising base stations 9-15. A mobile

communication device 16 is comprised in the radio zone 7. The mobile communication device 16 may be a cell phone or handset, or any other suitable mobile communication device. In the example given, the system 1 is a direct sequence spread spectrum system, and the mobile communication device 16 comprises a rake receiver as shown in further detail in
5 Figure 3. Groups of radio base stations are coupled to switching centers (not shown), and the switching centers are coupled to each other.

Figure 2 shows resolved components 20-22 of a multi-path signal, and early/late signals E and L. Upon initial synchronization of the mobile communication device 16 to the system, at power-on of the device 16, a searcher (not shown in detail) resolves the
10 components 20-22 from the system 1, and allocates the resolved components 20-22 to rake fingers of the rake receiver. Such initial synchronization is well known in the art. Thereafter, the rake fingers adopt a tracking mode synchronization wherein each rake finger is aligned and is kept aligned to its resolved component. The early/late signals E and L represent respective current situations wherein a rake finger receives a multi-path component early or
15 late with respect to an optimum reception time of maximum signal energy 23.

Figure 3 shows the communication device 16 with a rake finger 30 in such a rake receiver according to the invention. The rake receiver diversity combines resolved components of a multi-path signal to form a diversity combined signal that is supplied to a symbol detector. The communication device 16 comprises a radio transmission and reception
20 front end 31 and a plurality of rake fingers of which the rake finger 30 is shown. The radio front end 31 provides the usual reception, down-mixing, signal sampling, and transmission tasks, and provides a complex input signal 32 to the rake fingers, a sampled base band signal. In principle, the complex input signal can also be a low-intermediate frequency signal. A transmission branch is indicated by Tx. For the purpose of the invention only the rake finger
25 30 is shown in further detail. A processing means processes the complex input signal 32. Such processing means could be hard-wired logic or could be DSP (Digital Signal Processor) firmware, or a software program. In the embodiment shown, the rake finger 30 comprises a complex variable delay arrangement 33 that delays the complex input signal over maximally 8 samples of the complex input signal 32, a chip containing 8 samples. The complex variable
30 delay 33 provides fractional-chip delay of the complex input signal 32. Once the correct fractional-chip delay has been applied, the delayed signal is immediately down-sampled to one sample per chip, by down-sampling means that decimate the delayed signal by eight. A down-sampled signal 35 is next multiplied by the complex conjugate of a complex PN (Pseudo-Noise) sequence 36 which is generated by a pseudo-noise generator 37. At chip-

boundary, the complex PN sequence is adjusted in phase to match the resolved component 22 in the complex input signal 32. A resulting de-scrambled signal 37 that is provided by a multiplier 38 is then multiplied by a multiplier 39 with an orthogonal variable spreading factor code (OVSF) generated by an OVSF sequence generator 41, such an OVSF code being equivalent to a Walsh code. The phase of the OVSF code is also controlled by the shown delay locked loop, providing both fractional-chip and chip-boundary control signals. Next, a sliding integrator 42 provides a sliding integration over the length of the OVSF code 40, in the embodiment given over sixty-four chips. After integration, a complex variable delay 43 provides delay equalization to the nearest integer number of symbols, before decimation by sixty-four to the symbol rate by down-sampling means 44. As usual, and finally, to produce an output, a de-spread signal 45 is multiplied by the complex conjugate of a channel tap estimate obtained from a pilot channel broadcast by a base station, e.g., the base station 14. Timing control means 46 provides delay control signals to the complex variable delays 33 and 43, and phase control signals to the PN sequence generator 37 and to the OVSF sequence generator 41. The rake finger 30 further comprises an early/late detector 47 that provides power estimate signals of the early and late signals E and L to the timing control means 46.

Figure 4 shows the early/late detector 47 in the rake finger 30 of the mobile communication device 16 according to the invention. The early/late detector 47 has respective early and late branches 60 and 61. The early/late-timing detector 47 is used to derive a feedback signal for the timing loop. Two decimation-by-eight operations are done by respective down-samplers 62 and 63, at different timing offsets. The timing offsets are chosen at a sample separation of a fraction of a chip. Both early and late branches 60 and 61 are de-scrambled by multiplication with the complex conjugate of the scrambling PN sequence, by respective multipliers, and then respectively integrated over a finite period using integrate-and-dump operations 66 and 67. The complex magnitude squared is then taken in both branches 60 and 61, by squarer arrangements 68 and 69 to enable subsequent non-coherent integration by means of further integrate-and-dump operations 70 and 71 providing power estimate signals 72 and 73 of the early and late signals E and L. A timing error signal e is derived in the processing block 74 using the following logic: if three times the power estimate signal of the signal E is greater than two times the power estimate signal of the signal L then $e=-1$, else if three times the power estimate signal of the signal L is greater than two times the power estimate signal of the signal E then $e=+1$, else $e=0$. There is thus a dead zone in the range $2/3 \leq \text{power estimate of E divided by power estimate of L} \leq 3/2$, \leq indicating smaller than or equal to. The timing error events of the early and late

signals are available from the output of the early/late detector 47 pulses 75, either positive or negative unit pulses depending on the direction of the error. The pulses 75 are counted in the timing control means 46 by properly configured up/down counters to derive the various timing control signals needed for the rake finger 30.

5 Figure 5 shows a counter arrangement in the rake finger 30 according to the invention. The counter arrangement comprises up/down counters 81, 82 and 83 which respectively provide control signals 84, 85 and 86. A counter carry signal 87 of the counter 81 is provided to a hold input of the counter 82 via an inverter 88, and a counter carry signal 89 of the counter 82 is provided to a hold input of the counter 83 via an inverter 90. The
10 positive and negative unit pulses 75 are separated by means of comparators 91 and 92, and supplied to respective up and down count inputs of the counters 81-83. The counters 81-83 are clocked according to an initial delay estimate (as provided through initial synchronization to the system 1). The initial estimate is loaded into a counter which then decrements to zero. During the time that the counter value is greater than zero, a control input to the counter
15 chain 81-83 and PN sequence generator 37 is held at logic '1' causing them to advance to the value which was preloaded. After this time, the control input is switched to the output of the early-late event detector 47. Equivalent functionality can be obtained by using presetable counters and a presetable PN sequencer. The up/down counters 81-83 are sample, chip and symbol counters, respectively, with cycle count values equal to the number of samples per
20 chip, the number of chips per symbol and the number of symbols per frame respectively. The output or control signals 84, 85 and 86 are thus a sample delay control signal which controls the complex variable delay 33 at fractional-chip delay, a chip delay control signal which controls the slewable OVFSF sequence generator 41, and a symbol delay control signal which is used outside the rake finger 30 for symbol alignment prior to maximal ratio combining of
25 output signals of different rake fingers. The PN sequence generator 37 is a complex conjugate PN source containing slewable PN generators which form the real and imaginary parts of the complex PN source. The complex conjugate is obtained by negating the polarity of the imaginary output. The PN generator blocks accept a control input of +1 or -1 to advance or retard the generator phase by one chip, i.e., the PN generator is only shifted when
30 the sample clock rolls over from one chip to another.

Once the values of the sample delay control signal, the chip delay control signal, and the symbol delay control signal are available, it becomes possible to derive the timing control values needed inside the rake finger 30. The following equations are implemented in the timing control means:

- the complex variable delay 33 is set to $\delta_1 = N_s - 1$ - value of the sample delay control signal, where N_s is the number of samples per chip;
- the phase of the slewable OVVSF generator 41 is set to minus the value of the chip delay control signal;
- 5 - the complex variable delay 43 is set to $= N_w - 1$ - value of the chip delay control signal, where N_w is the number of chips per Walsh symbol; and
- the total delay computed by the rake finger 30 is:
- $d_{total} =$ value of the sample delay control signal + N_s times the value of the chip delay control signal + N_s times N_w times the value of the symbol delay control signal.

10 In the described embodiment, an oversampling rate of between four and eight samples is used. In another embodiment, using adjustable FIR-filters to produce the timing delay, the oversampling rate and thereby power consumption is advantageously reduced.

Figure 6 shows an adjustable digital FIR filter 100 in another embodiment of the rake finger 30 according to the invention. The filter 100 is used to at least produce a part
 15 of the fractional-chip or sub-chip delay. To this end the bulk delay of the filter 100 is selected. In this way a rake finger is built which requires only two or four samples per chip at its input. Depending on the architecture of analog-converters contained in the front-end 31 and the receiver's tolerance to aliasing, the maximum sampling rate used by the CDMA receiver could thereby be reduced. In the embodiment shown, the adjustable digital FIR
 20 (Finite Impulse Response) filter 100 has four filter stages 101-104 with a pre-computed set of FIR tap coefficients 105-108 which set tap weights 109-112 of the filter 100. Using a summing stage 113, outputs of the weighted filter stages are summed to produce a filter output signal 114.

Figure 7 shows a look-up table 120 with entries of filter tap coefficients 105-
 25 108 for the FIR filter 100, for a desired bulk delay. Each set of FIR filter coefficients has a pre-determined group delay while acting as a low pass filter. The FIR filter coefficients are directly synthesized using an inverse Fast Fourier Transform from the desired response. For easy of calculation, the frequency response is assumed to be an ideal low pass filter with a cliff-edge at half the Nyquist frequency. The phase is assumed to be linear with the slope
 30 depending on the required group delay.

Using the above principles, the following is an example of filter coefficients suitable for time shifting.

0.2207	0.3560	0.3560	0.2207	0.0293
0.1976	0.3455	0.3642	0.2428	0.0524
0.1738	0.3329	0.3702	0.2639	0.0762
0.1495	0.3183	0.3738	0.2836	0.1005
0.1250	0.3018	0.3750	0.3018	0.1250
0.1005	0.2836	0.3738	0.3138	0.1495
0.0762	0.2639	0.3702	0.3329	0.1738
0.0524	0.2428	0.3642	0.3455	0.1976
0.0293	0.2207	0.3560	0.3560	0.2207

Figure 8 shows a clocked controllable shift register 130 in the rake finger 30 according to the invention, as an embodiment of a real part of the complex variable delay 33.

- 5 The register 130 has eight shift register sections. The shift register maximally contains eight samples of the input signal 32. In order to generate the desired fractional-chip delay, an output 131 of the register 130 is coupled to an appropriate shift register section.

- In view of the foregoing it will be evident to a person skilled in the art that various modifications may be made within the spirit and the scope of the invention as
 10 hereinafter defined by the appended claims and that the invention is thus not limited to the examples provided. The word "comprising" does not exclude the presence of other elements or steps than those listed in a claim.

CLAIMS:

1. A method of tracking a resolved component (20-22) of a multi-path signal (32) assigned to a rake finger (30) of a spread spectrum rake receiver, said method comprising:
 - variably delaying (33) said resolved component;
 - performing an early-late detection (47) on said variably delayed resolved component so as to determine whether said resolved component arrived early (E) or late (L) with respect to an optimum arrival time (23), and generating a first pulse (75) if said early-late detection determines that said resolved component arrived early and generating a second pulse if said early-late detection determines that said resolved component arrived late;
 - counting (81, 82, 83) said first and second pulses (75), said first pulse causing counting in a first direction and said second pulse causing counting in a second direction;
 - deriving from said counting a fractional-chip delay timing adjustment signal (84), and feeding back said derived fractional-chip delay timing adjustment signal to adjust said variably delaying (33) of said resolved component (20-22), and
 - deriving from said counting a chip delay phase adjustment signal (85), and feeding back said derived chip delay phase adjustment signal (85) to control a phase of a pseudo-noise generator (37).
2. A method as claimed in Claim 1, doing said variably delaying (33) over maximally a number of samples per chip in said complex input signal (32), and generating said chip delay phase adjustment signal (85) by counting carry signals (87) from fractional-chip counting (81) during said counting, said fractional-chip counting causing said carry signals at a counting value representative of said number of samples per chip.
3. A method as claimed in Claim 2, generating said fractional-chip delay timing adjustment signal (84) from said fractional-chip counting (81).
4. A method as claimed in Claim 1, performing said variably delaying (33) by controlling a shift register (130) using said fractional-chip delay timing adjustment signal (84).

5. A method as claimed in Claim 1, performing said variably delaying (33) by controlling a delay of a digital filter register (100) using said fractional-chip delay timing adjustment signal (84).

5

6. A rake receiver comprising:

- a rake finger (30) of a spread spectrum rake receiver, said rake finger (30) tracking a resolved component (20-22) of a multi-path signal (32) assigned to said rake finger (30), said rake finger (30) comprising:
- 10 - means for variably delaying (33) said resolved component (20-22);
- means for performing an early-late detection (47) on said variably delayed resolved component (20-22) so as to determine whether said resolved component arrived early (E) or late (L) with respect to an optimum arrival time (23), and means for generating (74) a first pulse if said early-late detection determines that said resolved component arrived
- 15 early and means for generating a second pulse if said early-late detection determines that said resolved component arrived late;
- means for counting (81, 82, 83) said first and second pulses (75), said first pulse causing counting in a first direction and said second pulse causing counting in a second direction;
- means for deriving from said counting a fractional-chip delay timing adjustment signal
- 20 (84), and for feeding back said derived fractional-chip delay timing adjustment signal to adjust said variably delaying (33) of said resolved component (20-22), and
- means for deriving from said counting a chip delay phase adjustment signal (85), and for feeding back said derived chip delay phase adjustment signal (84) to control a phase of a pseudo-noise generator (37).

25

7. A rake receiver comprising:

- a rake finger (30) of a spread spectrum rake receiver, said rake finger (30) tracking a resolved component (20-22) of a multi-path signal (32) assigned to said rake finger (30), said rake finger comprising:
- 30 - a variable delay arrangement (33) configured to delay said resolved component (20-22);
- an early-late detector (47) configured to perform an early-late detection on said variably delayed resolved component so as to determine whether said resolved component arrived early (E) or late (L) with respect to an optimum arrival time (23), and to generate a first pulse if said early-late detection determines that said resolved component arrives early

and to generate a second pulse if said early-late detection determines that said resolved component arrives late;

- an adjustable pseudo-noise generator (37) for generating a pseudo-noise sequence for de-scrambling said resolved component;
- 5 - a first counter (81) configured to count said first and second pulses (75), said first counter (81) providing a fractional-chip delay timing adjustment signal (84) to said variable delay arrangement (33) in order to provide time alignment of said rake finger (30) with said resolved component (20-22); and
- a second counter (82) configured to count carry signals (87) generated by said first
10 counter (81), said second counter (82) providing a chip delay phase adjustment signal (85) to said adjustable pseudo-noise generator (37) in order to provide phase alignment of said rake finger with said resolved component.

8. A rake receiver as claimed in Claim 10, wherein said variable delay
15 arrangement (33) is a shift register (130), or a digital filter (100) with an adjustable delay, which is set through selection of filter coefficients (109-112), wherein said filter coefficients (109-112) are selected from a look-up table (120) comprised in said rake receiver, said look-up table having entries of filter coefficients corresponding to predetermined delays.

20 9. A rake receiver as claimed in Claim 10, wherein said variable delay arrangement is a combination of a shift register and a digital filter with an adjustable delay.

10. A spread spectrum communication system (1) having a plurality of cells (2-8) with base stations (9-15) covering said cells, with a mobile communication device (16) for
25 communicating with one of said base stations (9-15), said mobile communication device (16) having a rake receiver with a rake finger (30), said rake finger (30) tracking a component (20-22) of a multi-path signal (32) assigned to said rake finger (30), said rake finger (30) comprising:

- means for variably delaying (33) said resolved component (20-22);
- 30 - means for performing an early-late detection (47) on said resolved component (20-22) so as to determine whether said resolved component arrived early (E) or late (L) with respect to an optimum arrival time (23), and means (74) for generating a first pulse if said early-late detection determines that said resolved component arrived early and means for

generating a second pulse if said early-late detection determines that said resolved component arrived late;

- means for counting (81, 82, 83) said first and second pulses (75), said first pulse causing counting in a first direction and said second pulse causing counting in a second direction;
- 5 - means for deriving from said counting a fractional-chip delay timing adjustment signal (84), and for feeding back said derived fractional-chip delay timing adjustment signal (84) to adjust said variably delaying (33) of said resolved component (20-22), and
- means for deriving from said counting a chip delay phase adjustment signal (85), and for feeding back said derived chip delay phase adjustment signal (85) to control a phase of a
- 10 pseudo-noise generator (37).

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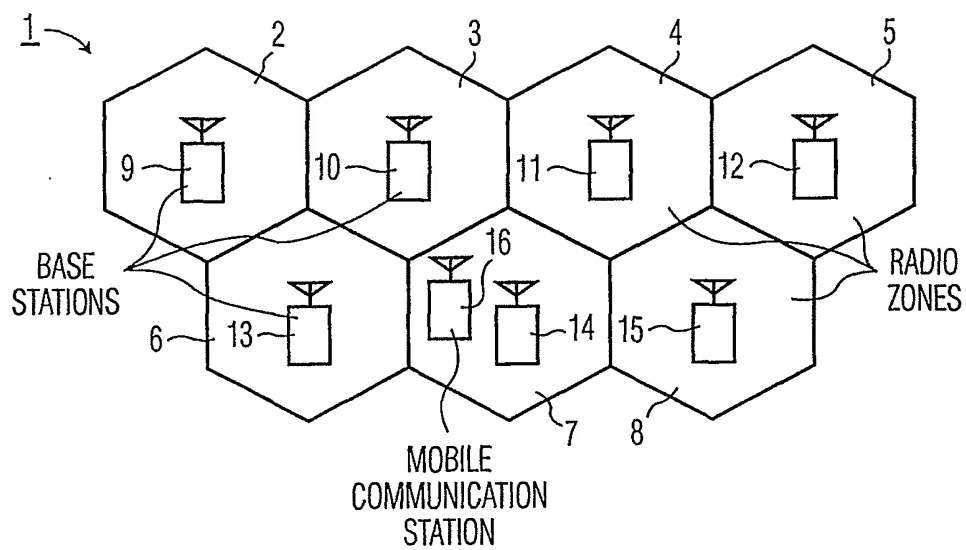


FIG. 1

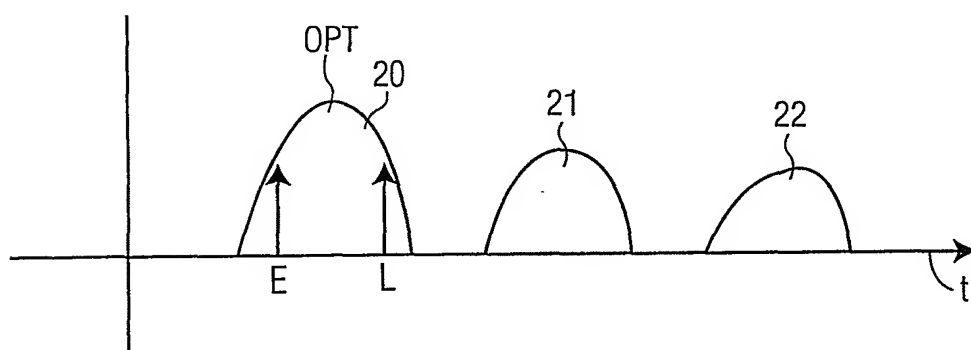


FIG. 2

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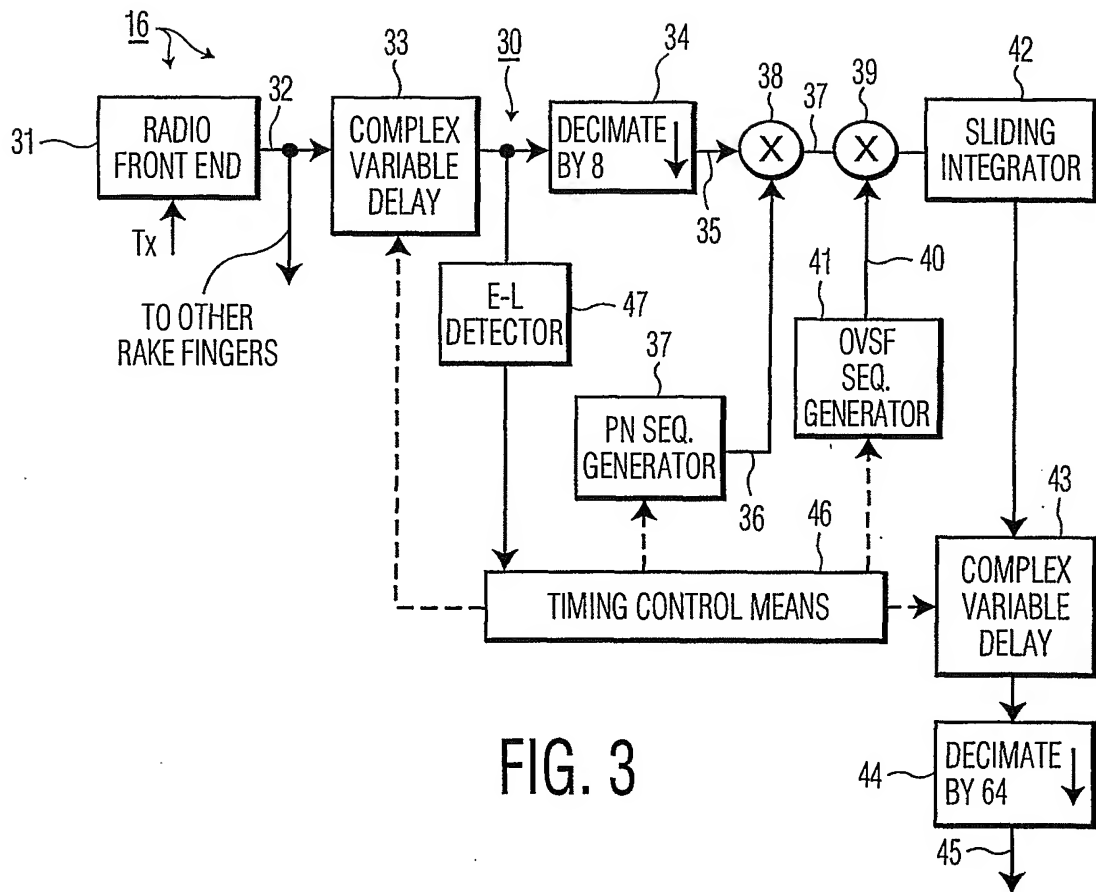


FIG. 3

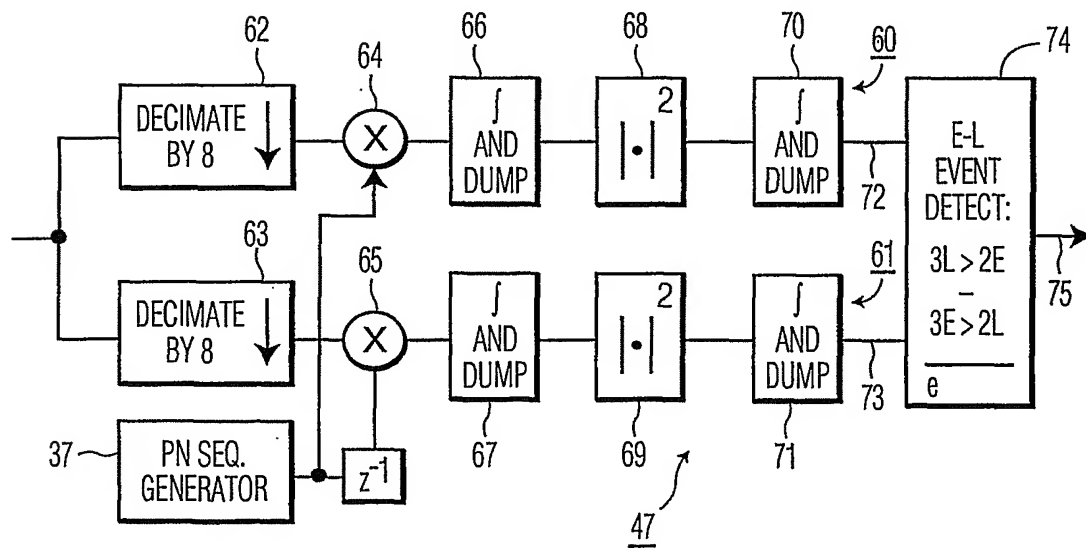


FIG. 4

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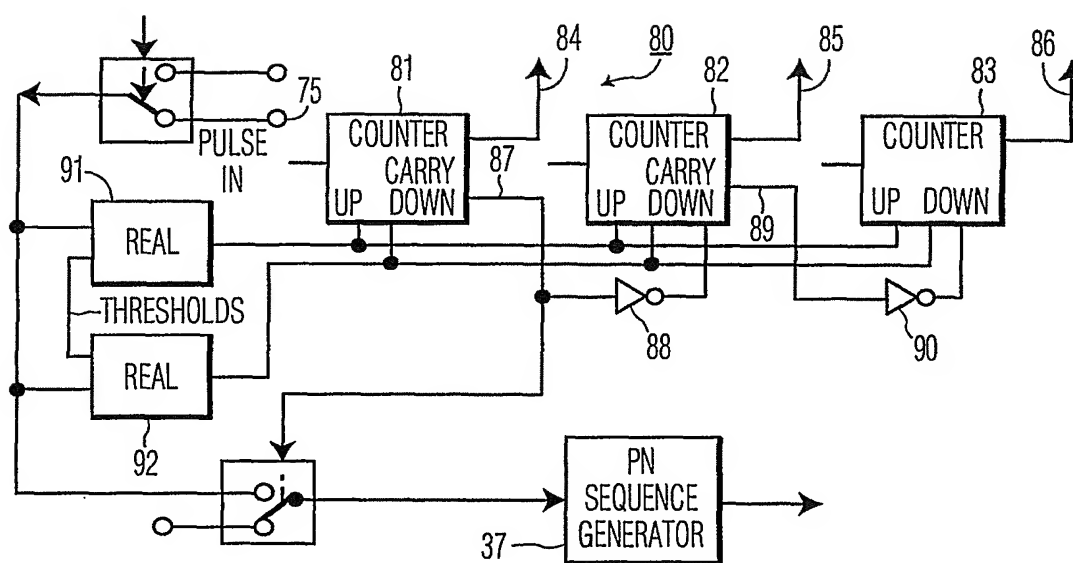


FIG. 5

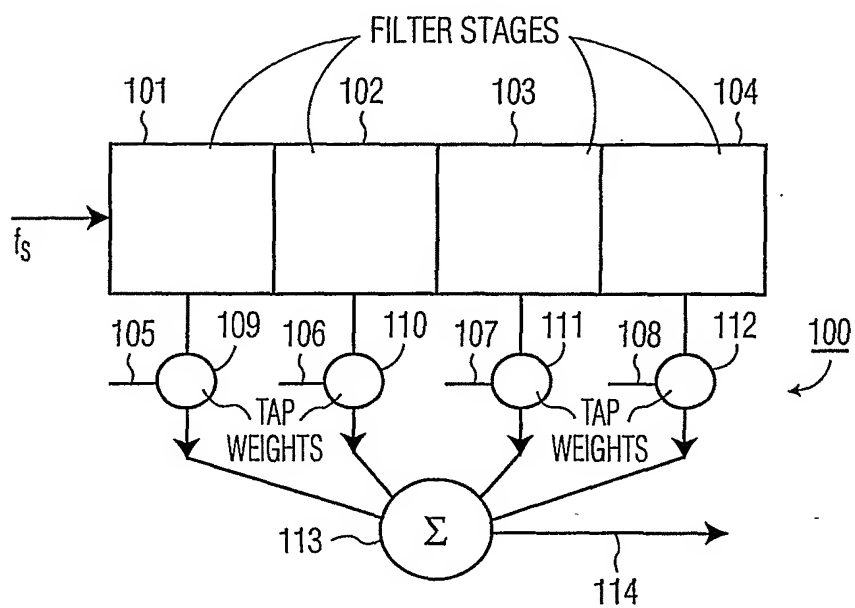


FIG. 6

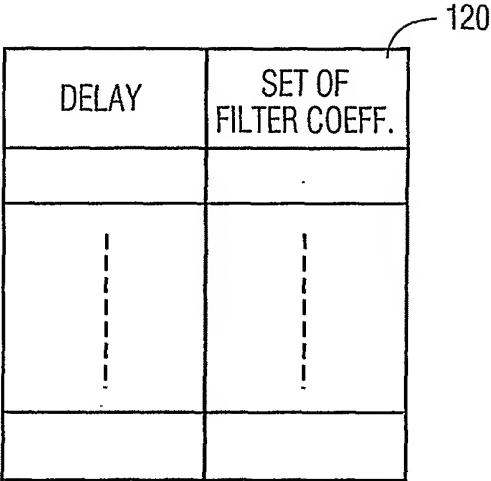


FIG. 7

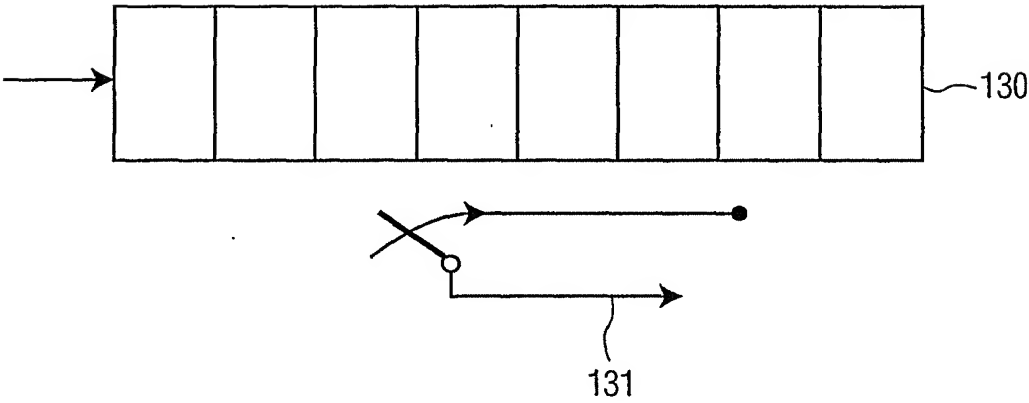


FIG. 8